IN THE CLAIMS:

Please amend claims 1 and 8-10, and add new claims 17-19 as shown in the attached sheet(s).

REPLACEMENT CLAIMS

Please substitute the following claims for the pending claims with the same number.

Sub B17

A1

1. (Amended) A method of making a semiconductor device, the method comprising the steps of:

mounting a semiconductor chip on a lower conductor, with first solder material applied between the chip and the lower conductor;

positioning an upper conductor on the chip, with second solder material applied between the chip and the upper conductor;

heating up the first and the second solder materials beyond melting points of the respective materials; and

solidifying the first and the second solder materials; wherein the first solder material is caused to solidify earlier than the second solder material in the solidifying step.

8. (Amended) The method according to claim 6, wherein the upper conductor comprises upper lead portions [divided into first and second groups].

A2

Sub B17

9. (Amended) The method according to claim 14, further comprising the step of removing at least one of the lower and the upper lead portions from the frame.

10. (Amended) The method according to clam 14, wherein the frame comprises first and second common bars parallel to each other, the upper lead portions being divided into first

A2

and second groups, the upper lead portions in the first group extending from the first common bar toward the second common bar, the upper lead portions in the second group extending from the second common bar toward the first common bar.

17. (New) The method according to claim 1, further comprising the step of preparing a conductive frame which includes a first conductive pattern and a second conductive pattern, the first conductive pattern including the lower conductor, the second conductive pattern including the upper conductor.

A3
Sub B7

18. (New) The method according to claim 12, wherein the lower conductor comprises a die pad portion and lower lead portions extending from the die pad portion on which the semiconductor chip is to be mounted.

19. (New) The method according to claim 13, wherein the second conductive pattern comprises upper lead portions at least one of which is to be connected to the semiconductor chip as the upper conductor.